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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,837	03/15/2004	David A. Klein	200309347-2	1528

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EXAMINER	
CERULLO, JEREMY S	
ART UNIT	**PAPER NUMBER**
2111	

NOTIFICATION DATE	DELIVERY MODE
01/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/800,837	KLEIN ET AL.	
	Examiner	Art Unit	
	Jeremy S. Cerullo	2111	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,13,14,16-31 and 33-47* is/are rejected.

7)☒ Claim(s) *8-12,15 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20071026*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-47 are pending in the following action.

Response to Arguments

2. Applicant's arguments filed 25 May 2007 have been fully considered but they are not persuasive.

3. Regarding the applicant's arguments against the rejection of Claims 1-4, 13-14, 16-17, 20-26, 33-34, 36-38, and 40-44 are rejected under 35 U.S.C. 103(a), the examiner respectfully disagrees. It appears that the applicant still misunderstands the way in which the art has been applied. The combination of references given is used to reject the invention of Claims 1-4, 13-14, 16-17, 20-26, 33-34, 36-38, and 40-44 as a whole. Therefor the reasoning provided is for combining the references to achieve the complete invention, not just the invention in the independent claims. Once again, for clarification, an in-depth mapping of which references are relied upon for the limitations of each claim is provided in the rejection below.

4. Regarding the applicant's arguments concerning the double patenting rejections of Claims 5-7, 18-19, 27-31, 35, and 39, the examiner disagrees. The applicant argues that the examiner does not point out the differences between the instant application and the claim in the patent. In the rejection below, the examiner states what the patent does not teach and gives secondary references that render the instant invention obvious.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-4, 13-14, 16-17, 20-26, 33-34, 36-38, 40-44, and 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,761,516 ("Rostoker" et al.), U.S. Patent No. 7,079,386 ("Jochym" et al.), and U.S. Patent Application Publication No. 2003/0088800 ("Cai") in view of what is old and well known in the art.

8. Rostoker teaches (Abstract; Figure 2; Column 3, Lines 9-58) an apparatus, a system comprising the apparatus, and a method for using the apparatus comprising a

single-chip module (designed to replace a single processor module, having the same size and footprint), connected to a computer system as a single processor, comprising a plurality of processors processing data independently and simultaneously, cache control and bus bridge device (memory control / IO control) between the processors and the system bus (memory bus / IO bus) [as claimed in Claims 1, 3, 16, 17, 25, 26, 27, 29, 30, 33, 34, 36, 37, 40, 41, 44, 46, and 47]. Rostoker does not teach the use of a fourth level shared cache in multiprocessor system [as claimed in Claims 29 and 43] or a method in a multiprocessor system for regulating the power consumption of a system by adjusting the operating frequencies of the processors [as claimed in Claims 20-24]. However, Jochym teaches (Column 5, Lines 15-25) the use of a fourth level shared cache in a multiprocessor system [Claims 29 and 43] and Cai teaches (Paragraphs [0005]-[0007]) a multiprocessor system that comprises a method for regulating the power consumption of the system by adjusting the operating frequencies of the processors while maintaining an overall level of system performance [Claims 20-24]. Also, Rostoker teaches (Column 3, Lines 9-16) that while the examples use Motorola and Intel X86 processors, invention is not limited to any particular combination of processors, but does not explicitly teach the use of Intel Itanium processors [as claimed in Claims 2, 4, and 38]. The examiner takes OFFICAL NOTICE that Intel Itanium processors are well known in the art [Claims 2, 4, and 38], that it is well known in the art to include multiple processor modules in a computer system [Claim 14], and that it is well known to include power cabling in a computer system [Claim 13]. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used

the teachings of Rostoker, Jochym, and Cai using Itanium processors to create a power-efficient multiprocessor system on a single processor-style module.

9. Regarding Claim 1, the claimed elements are taught in the combination of references above as follows:

a. Plurality of logically independent processors (Rostoker: Figure 2, Items 54 and 56)

b. System bus (Rostoker: Figure 2, Item 62)

c. Cache control and bus bridge device (Rostoker: Figure 2, Items 58 and 60)

d. Processors and cache control and bus bridge device in a module form such that the module is a drop-in replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

10. Regarding Claim 2, the claimed elements are taught in the combination of references above as follows:

e. Processors are IPF processors (Official Notice: Intel Itanium processors are well known in the art)

11. Regarding Claim 3, the claimed elements are taught in the combination of references above as follows:

f. Processors and cache control and bus bridge device in a module form such that the module is a drop-in replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

12. Regarding Claim 4, the claimed elements are taught in the combination of references above as follows:

g. Processor module is an Itanium module are IPF processors (Official Notice: Intel Itanium processors are well known in the art)

13. Regarding Claim 13, the claimed elements are taught in the combination of references above as follows:

h. Use of flexible power cable within the module (Official Notice: it is well known in the art to include flexible power cabling in a computer system)

14. Regarding Claim 14, the claimed elements are taught in the combination of references above as follows:

i. Plurality of similar apparatuses in computing device (Official Notice: it is well known in the art to include multiple processor modules in a computer system)

15. Regarding Claim 16, the claimed elements are taught in the combination of references above as follows:

j. Plurality of logically independent processors (Rostoker: Figure 2, Items 54 and 56)

k. System bus (Rostoker: Figure 2, Item 62)

l. Cache control and bus bridge device (Rostoker: Figure 2, Items 58 and 60)

m. Processors and cache control and bus bridge device in a module form such that the module is a drop-in replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

n. Processors process data independently (Rostoker: Column 3, Lines 42-52)

16. Regarding Claim 17, the claimed elements are taught in the combination of references above as follows:

o. Module is a drop-in replacement (connects to a system board) for a single processor module (Rostoker: Column 3, Lines 4-52)

p. Use of a system bus (Rostoker: Figure 2, Item 72)

q. Processors process data independently (Rostoker: Column 3, Lines 42-52)

17. Regarding Claim 20, the claimed elements are taught in the combination of references above as follows:

r. Power consumption equal to or less than that of a standard single processor module (Cai: Paragraphs [0002]-[0007])

18. Regarding Claim 21, the claimed elements are taught in the combination of references above as follows:

s. Changing from a multi-issue mode to a single issue mode (disabling one of the processing units) (Cai: Paragraph [0006])

19. Regarding Claim 22, the claimed elements are taught in the combination of references above as follows:

t. Lowering operating frequency (Cai: Paragraphs [0005] and [0015])

20. Regarding Claim 23, the claimed elements are taught in the combination of references above as follows:

u. Performance better than standard single-processor module (Cai: Paragraphs [0015]-[0018])

21. Regarding Claim 24, the claimed elements are taught in the combination of references above as follows:

v. Performance per unit power optimized (Cai: Paragraphs [0015]-[0018])

22. Regarding Claim 25, the claimed elements are taught in the combination of references above as follows:

w. Replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

23. Regarding Claim 26, the claimed elements are taught in the combination of references above as follows:

x. Volume not greater than that of single processor module (designed as a replacement) (Rostoker: Column 3, Lines 4-52)

24. Regarding Claim 33, the claimed elements are taught in the combination of references above as follows:

y. Plurality of logically independent processors (Rostoker: Figure 2, Items 54 and 56)

z. System bus (Rostoker: Figure 2, Item 62)

aa. Cache control and bus bridge device (Rostoker: Figure 2, Items 58 and 60)

bb. Processors and cache control and bus bridge device in a module form such that the module is a drop-in replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

25. Regarding Claim 34, the claimed elements are taught in the combination of references above as follows:

cc. Volume not greater than that of single processor module (designed as a replacement) (Rostoker: Column 3, Lines 4-52)

26. Regarding Claim 36, the claimed elements are taught in the combination of references above as follows:

dd. Plurality of logically independent processors (Rostoker: Figure 2, Items 54 and 56)

ee. Cache control and bus bridge device (Rostoker: Figure 2, Items 58 and 60)

ff. System bus (Rostoker: Figure 2, Item 72)

gg. Cache control and bus bridge device adapted to communicate with components such that the multiple processors are a single processor module (Rostoker: Column 3, Lines 4-52)

27. Regarding Claim 37, the claimed elements are taught in the combination of references above as follows:

hh. Processors and cache control and bus bridge device in a module form such that the module is a drop-in replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

28. Regarding Claim 38, the claimed elements are taught in the combination of references above as follows:

ii. Processors are IPF processors (Official Notice: Intel Itanium processors are well known in the art)

29. Regarding Claim 40, the claimed elements are taught in the combination of references above as follows:

jj. Processors and cache control and bus bridge device in a module form such that the module is a drop-in replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

30. Regarding Claim 41, the claimed elements are taught in the combination of references above as follows:

kk. Plurality of logically independent processors (Rostoker: Figure 2, Items 54 and 56)

ll. Processors and cache control and bus bridge device in a module form such that the module is a drop-in replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

mm. Processors process data independently (Rostoker: Column 3, Lines 42-52)

nn. Module is a drop-in replacement (connects to a system board) for a single processor module (Rostoker: Column 3, Lines 4-52)

oo. Use of a system bus (Rostoker: Figure 2, Item 72)

pp. Processors process data independently (Rostoker: Column 3, Lines 42-52)

31. Regarding Claim 42, the claimed elements are taught in the combination of references above as follows:

qq. Power consumption equal to or less than that of a standard single processor module (Cai: Paragraphs [0002]-[0007])

32. Regarding Claim 43, the claimed elements are taught in the combination of references above as follows:

rr. Fourth-Level Cache (Jochym: Column 5, Lines 15-25)

33. Regarding Claim 44, the claimed elements are taught in the combination of references above as follows:

ss. Replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

34. Regarding Claim 45, the claimed elements are taught in the combination of references above as follows:

tt. System comprises multi-processor modules (Rostoker: Column 3, Lines 33-42)

35. Regarding Claim 46, the claimed elements are taught in the combination of references above as follows:

uu. Cache control and bus bridge device adapted to communicate with components such that the multiple processors are a single processor module (Rostoker: Column 3, Lines 4-52)

Double Patenting

36. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Omum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

37. Claims 5-7, 18-19, 27-31, 35, and 39 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-9 of U.S. Patent No. 7,072,185 ("Belady" et al.) in view of Rostoker, Jochym, and Cai as applied to Claims 1-4, 16-17, 20-26, 33-34, 36-38, and 40-44, U.S. Patent No. 5,805,915 ("Wilkinson" et al.), and what is old and well known in the art.

38. As for Claims 5-7, 18, 27, 29-30, 35, 39, and 45 Belady teaches the mechanical arrangement and construction of the limitations of Claims 5-7, 11, 18, 27, 29-30, 35, 39, and 45 of the instant application, but Belady does not teach electronically functional elements as claimed. However, Rostoker, Jochym, and Cai disclose the electronically functional elements (See Rejection of Claims 1-4, 16-17, 20-26, 33-34, 36-38, and 40-44 above). One of ordinary skill in the art, when constructing a system based on the teachings of Belady, would have looked to the electrical arts to determine the appropriate electrical techniques needed to produce a complete system, and would have found the teachings of Rostoker, Jochym, and Cai.

39. As for Claim 19, it is inherent that in order to have a power supply with more components in the same volume, the components would have to be more densely packed.

40. As for Claim 28, the examiner takes OFFICIAL NOTICE that it is old and well known in the art to incorporate multi-processor modules in servers, and it would have been obvious to one of ordinary skill in the art at the time of the invention to have placed the multi-processor module in a computer server.

41. As for Claim 31, Wilkinson teaches the use of wedgelock devices to secure processor modules (Figure 5). It would have been obvious to one of ordinary skill in the art at the time of the invention to have used wedgelock devices as taught by Wilkinson in order to provide a secure connection between the processors and the computer system.

42. Claim 1 of Belady is also found to be obvious over Claim 7 of the instant application. Claim 1 of Belady is anticipated by Claim 7 of the instant application in that Claim 7 of the instant application contains all of the limitations of Claim 1 of Belady. The module of Belady is equivalent to the power board of the instant application. One side of the power board contacts the processor board (PCB of Belady) and the other side contacts a heat spreader (thermal dissipation device of Belady) wherein pedestals of the heat spreader pass through the power board to contact the processor board (pass-thru holes of Belady). Claim 1 of Belady therefore is not patentably distinct from Claim 7 of the instant application.

Allowable Subject Matter

43. Claims 8-12, 15, and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (571)

272-3634. The examiner can normally be reached on Monday - Thursday, 8:00-4:00; Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JSC/
Jeremy S. Cerullo
Examiner

PAUL R. MYERS
PRIMARY EXAMINER